

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			ATTY. DOCKET NO. <b>32796</b>		SERIAL NO.	
<b>INFORMATION DISCLOSURE CITATION BY APPLICANT</b> <i>(USE SEVERAL SHEETS IF NECESSARY)</i>					APPLICANT: <b>Hidetoshi Narahara et al.</b>			
					FILING DATE: <b>July 7, 2000</b>		GROUP ART UNIT:	

  

U.S. PATENT DOCUMENTS							
Examiner Initial	Document No.	Date	Name	Class	Subclass	Filing Date if Appropriate	
KAN	A	5,117,377	Finman	703	2	1c564 U.S. PTD 09/07/00 	
KAN	B	5,479,440	Esfahani	375	346		
	C						
	D						
	E						
	F						
	G						
	H						
FOREIGN PATENT DOCUMENTS							
	Document No.	Date	Country	Class	Subclass	Translation	
	I						
	J						
	K						
	L						
	M						
OTHER REFERENCES <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>							
KAN	N	Analog Integrated Circuits and signal Processing, 14, pp. 113-129 (1997), di/dt Noise in CMOS Integrated Circuits, Patrik Larsson.					
KAN	O	EMI-Noise Analysis under ASIC Design Environment, Sachio Hayashi & Masaaki Yamada, DA Development Dept., Semiconductor DA & Test Engineering Center, Toshiba Corporation, pp. 16-21.					
KAN	P	IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B. Vol. 21, No. 3, August 1998, Interconnect and Circuit Modeling Techniques for Full-Chip Power Supply Noise Analysis, Howard H. Chen and J. Scott Neely, pp. 209-215.					
KAN	Q	Power Supply Noise Analysis Methodology for Deep-Submicron VLSI Chip Design, Howard H. Chen and David D. LingDAC97, Anaheim, California, (c)1997, pp. 1-6.					
Examiner:				Date Considered <b>10/25/03</b>			
<b>*Examiner:</b> Initial if reference considered, regardless of whether citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							